INFORMATION DISCLOSURE CITATION

PTO-1449

Date Mailed: **April 27, 1999**

Atty Docket 54355/253032	Serial No. 09/300,540 ~~Unassigned~~
Applicant Van Ginneken, et al.	
Filing Date ~~herewith~~ 4/27/99	Group Art Unit ~~Unassigned~~ 2825

U.S. PTO 09/300540 04/27/99 JC13

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
PV	5,757,657	05/26/98	Hathaway et al.	710	9	

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

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PV	Dion, J. and Monier, L.M.; "Countour: A Tile-based Gridless Router," *WRL Research Report* 3/95, Digital Western Research Laboratory
PV	Dion, J. and Monier, L.M.; "Recursive Layout Generation," *WRL Research Report* 2/95, Digital Western Research Laboratory

EXAMINER Phallaka Kik	DATE CONSIDERED 6/3/01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION PTO-1449 Date Mailed: October 20, 2000	Atty Docket 12907/253032	Serial No. 09/300,540
	Applicant Van Ginneken et al. [MAG-005]	
	Filing Date 4/27/99	Group Art Unit ~~2764~~ 2825

OIPE JC116 OCT 25 2000 PATENT & TRADEMARK OFFICE

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PV	Hwang., J., et al., "Generating layouts for self-emplementing modules"; Intl Workshop on Field Programmable Logic and Applications, FPGAS, GB, Abingdon, 31 Aug 1998, pp. 525-529
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PV	Fcanha, H.S.;, "Data astructtures for physical representation of VLSI," Software Eng'g Journal, GB, IEE. London, Vol5, No.6, Nov. 1, 1990.

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